

The attached Appendix includes marked-up copies of the specification
(37 C.F.R. §1.125(b)(2)) and each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Prompt and favorable examination on the merits is respectfully requested.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/gam

Attachments:

Substitute Abstract
Appendix
Substitute Specification
Marked-up copy of specification

Date: October 16, 2001

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

<p>DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry; Charge any fee due to our Deposit Account No. 15-0461</p>
--

APPENDIX

Changes to Abstract:

The following is a marked-up version of the amended Abstract:

A ferroelectric memory according to the present invention includes a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged, and a peripheral circuit for the passive matrix array. The passive matrix array is formed of a passive matrix array microchip, and the peripheral circuit, such as a word line driver circuit or a bit line driver circuit, is formed on a peripheral circuit substrate, thereby integrating the passive matrix array microchip on the peripheral circuit substrate. Since this structure allows the passive matrix array and the peripheral circuit therefor to be separately fabricated, the peripheral circuit is not adversely affected when fabricating the passive matrix array, thereby decreasing the degree of limitation in the fabrication process.

Changes to Specification:

A Substitute Specification is attached in accordance with 37 C.F.R. 1.125(b)(2).

Changes to Claims:

Claims 20-26 are added.

The following are marked-up versions of the amended claims:

1. (Amended) A ferroelectric memory, comprising:

a microstructure;

a passive matrix array ~~in which~~ that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the microstructure; ~~are arranged; and~~

a substrate, the microstructure being integrated on the substrate; and

a peripheral circuit for the passive matrix array, the peripheral circuit being formed on the substrate. wherein:

- ~~—— the passive matrix array is formed on a microstructure;~~
- ~~—— the peripheral circuit is formed on a substrate; and~~
- ~~—— the microstructure is integrated on the substrate.~~

2. (Amended) A ferroelectric memory, comprising:

a substrate;

a passive matrix array ~~in which~~ that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the substrate; are arranged; and

a microstructure; and

a peripheral circuit for the passive matrix array, ~~wherein:~~ the peripheral circuit being formed on the microstructure,

~~the passive matrix array is formed on a substrate;~~

~~the peripheral circuit is formed on a microstructure; and~~

~~the microstructures is being integrated on the substrate.~~

3. (Amended) A ferroelectric memory, comprising:

a first microstructure;

a passive matrix array ~~in which~~ that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the first microstructure; are arranged; and

a second microstructure;

a peripheral circuit for the passive matrix array, the peripheral circuit being formed on the second microstructure; and ~~wherein:~~

a substrate, the first and second microstructures being integrated on the substrate.

- ~~—— the passive matrix array is formed on a first microstructure;~~

~~the peripheral circuit is formed on a second microstructure; and~~

~~the first and second microstructures are integrated on a substrate.~~

4. (Amended) The ferroelectric memory according to claim 1, ~~2, or 3, wherein~~ further including a plurality of microstructures is integrated on the substrate. ~~in the case where the passive matrix array is formed on the microstructure, and a plurality of microstructures is integrated in the case where the peripheral circuits are formed on the microstructures.~~

5. (Amended) The ferroelectric memory according to claim 1, ~~as defined in any one of claims 1 to 4, wherein:~~

a recess portion in which the microstructure is provided is formed in the substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.

6. (Amended) The ferroelectric memory ~~as defined in~~ according to claim 5, wherein the substrate is formed by transfer-molding a photocurable resin.

7. (Amended) A ferroelectric memory, comprising:

a first microstructure;

a plurality of pairs of a passive matrix array in which that each includes memory cells formed of ferroelectric capacitors, the plurality of pairs of the passive matrix array being provided on the first microstructure ~~are arranged;~~

~~_____ a second microstructure;~~

a peripheral circuit for the passive matrix array, the peripheral circuit being formed on the second microstructure; and

~~_____ a plurality of pairs of the passive matrix array formed on a first microstructure and the peripheral circuit formed on a second microstructure,~~

a substrate, wherein at least one of the pairs is of the passive matrix array
being provided on each side of a the substrate.

8. (Amended) A ferroelectric memory, comprising:
a passive matrix array ~~in which~~ that includes memory cells formed of
ferroelectric capacitors ~~are arranged;~~
a peripheral circuit for the passive matrix array; ~~and~~
an associated circuit having ~~the a same~~ or a different function as the
~~ferroelectric memory cells; or a different function from the ferroelectric memory, wherein:~~
a single substrate; and
a plurality of microstructures, the passive matrix array, the peripheral circuit
and the associated circuit are being formed on each of a the plurality of microstructures, ; and
the microstructures are being integrated on a the single substrate.

9. (Amended) A ferroelectric memory, comprising:
a passive matrix array ~~in which~~ that includes memory cells formed of
ferroelectric capacitors; ~~are arranged; and~~
a peripheral circuit for the passive matrix array; and;
~~wherein a single microstructure,~~ the passive matrix array and the peripheral
circuit ~~are being~~ integrated on a the single microstructure.

10. (Amended) A ferroelectric memory, comprising:
a first microstructure;
a passive matrix array ~~in which~~ that includes memory cells formed of
ferroelectric capacitors, ~~are arranged; and~~ the passive matrix array being formed on the first
microstructure;
a second microstructure that is larger than the first microstructure, the first
microstructure being provided in a part of the second microstructure to be integrated; and

a peripheral circuit for the passive matrix array, the peripheral circuit being formed on the second microstructure.

~~—— the passive matrix array is formed on a first microstructure;~~

~~—— the peripheral circuit is formed on a second microstructure which is larger than the first microstructure; and~~

~~—— the first microstructure is provided in a part of the second microstructure to be integrated.~~

11. (Amended) A ferroelectric memory, comprising:

a plurality of microstructures;

a passive matrix array ~~in which~~ that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on each of the plurality of microstructures; are arranged; and

a peripheral circuit for the passive matrix array; ~~and, wherein:~~

~~—— the passive matrix array is formed on each of a plurality of microstructures;~~
and

a substrate, the microstructures are being provided in layers to be integrated in a the substrate.

12. (Amended) A method of fabricating a ferroelectric memory which includes: a passive matrix array ~~in which~~ including memory cells formed of ferroelectric capacitors, ~~are arranged;~~ and a peripheral circuit for the passive matrix array, ~~wherein:~~ the method comprising:

forming the passive matrix array is formed on a microstructure;

forming the peripheral circuit is formed on a substrate; and

integrating the microstructure is integrated on the substrate.

13. (Amended) A method of fabricating a ferroelectric memory which includes: a passive matrix array ~~in which including~~ memory cells formed of ferroelectric capacitors, ~~are arranged;~~ and a peripheral circuit for the passive matrix array, ~~wherein the method comprising:~~

forming the passive matrix array ~~is formed~~ on a substrate;

forming the peripheral circuit ~~is formed~~ on a microstructure; and

integrating the microstructure ~~is integrated~~ on the substrate.

14. (Amended) A method of fabricating a ferroelectric memory which includes: a passive matrix array ~~in which including~~ memory cells formed of ferroelectric capacitors, ~~are arranged;~~ and a peripheral circuit for the passive matrix array, ~~wherein the method comprising:~~

forming the passive matrix array ~~is formed~~ on a first microstructure;

forming the peripheral circuit ~~is formed~~ on a second microstructure; and

integrating the first and second microstructures ~~are integrated~~ on a substrate.

15. (Amended) The method of fabricating a ferroelectric memory as ~~defined in~~ any one of claims 12 to 14, ~~wherein according to claim 12, further including:~~

forming a substrate having a recess portion in the substrate which corresponds to a shape of the microstructure ~~is provided;~~ and

providing the microstructure ~~is provided~~ in the corresponding recess portion in the substrate to be integrated.

16. (Amended) The method of fabricating a ferroelectric memory as defined in claim 15,

wherein the step of providing the microstructure includes ~~is provided in the recess portion in the substrate by~~ providing a fluid which contains the microstructure to a surface of the substrate.

17. (Amended) A method of fabricating a ferroelectric memory which includes: a passive matrix array ~~in which~~ including memory cells formed of ferroelectric capacitors, ~~are arranged;~~ and a peripheral circuit for the passive matrix array, ~~wherein the method~~ comprising:

forming a plurality of pairs of the passive matrix array ~~formed~~ on a first microstructure; ~~and~~

forming the peripheral circuit ~~formed~~ on a second microstructure; ~~are provided;~~ and

integrating at least one of the pairs ~~is integrated~~ on each side of a substrate.

18. (Amended) A method of fabricating a ferroelectric memory, which includes: a passive matrix array ~~in which~~ including memory cells formed of ferroelectric capacitors, ~~are arranged;~~ and a peripheral circuit for the passive matrix array, ~~wherein the method~~ comprising:

forming the passive matrix array ~~is formed~~ on a first microstructure;

forming the peripheral circuit ~~is formed~~ on a second microstructure which is larger than the first microstructure; and

providing the first microstructure ~~is provided~~ in a part of the second microstructure to be integrated.

19. (Amended) A method of fabricating a ferroelectric memory, which includes: a passive matrix array ~~in which~~ including memory cells formed of ferroelectric capacitors, ~~are arranged;~~ and a peripheral circuit for the passive matrix array, ~~wherein the method~~ comprising:

forming the passive matrix array ~~is formed~~ on each of a plurality of microstructures; and

providing the microstructures ~~are provided~~ in layers to be integrated in a substrate.